**Domanda 1**

Considerando il processore MIPS64 e l’architettura descritta in seguito:

|  |  |  |
| --- | --- | --- |
| * + Integer ALU: 1 clock cycle   + Data memory: 1 clock cycle   + FP multiplier unit: pipelined 6 stages | * + FP arithmetic unit: pipelined 2 stages   + FP divider unit: not pipelined unit that requires 6 clock cycles   + branch delay slot: 1 clock cycle, and the branch delay slot disabled | * + forwarding enabled   + it is possible to complete instruction EXE stage in an out-of-order fashion. |

Usando il frammento di codice riportato, si calcoli il tempo di esecuzione dell’intero programma in colpi di clock e si completi la seguente tabella.

; for (i = 0; i < 100; i++) {

; v4[i] = v1[i] \* v2[i] \* v3[i];

; v5[i] = v1[i]+ v3[i]; }

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Clock cycles |
| .data |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| V1: .double “100 values” |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| V2: .double “100 values” |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| V3: .double “100 values”  …  V5: .double “100 zeros” |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| .text |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| main: daddui r1,r0,0 | F | D | E | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5 |
| daddui r2,r0,100 |  | F | D | E | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
| loop: l.d f1,v1(r1) |  |  | F | D | E | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
| l.d f2,v2(r1) |  |  |  | F | D | E | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
| mul.d f4,f1,f2 |  |  |  |  | F | D | s | \* | \* | \* | \* | \* | \* | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 7 |
| l.d f3,v3(r1) |  |  |  |  |  | F | S | D | E | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| mul.d f4,f4,f3 |  |  |  |  |  |  |  | F | D | s | s | s | s | \* | \* | \* | \* | \* | \* | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 6 |
| s.d f4,v4(r1) |  |  |  |  |  |  |  |  | F | s | s | s | s | D | E | s | s | s | s | s | M | W |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
| add.d f5,f1,f3 |  |  |  |  |  |  |  |  |  |  |  |  |  | F | D | s | s | s | s | s | + | + | M | W |  |  |  |  |  |  |  |  |  |  |  |  | 2 |
| s.d f5,v5(r1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | S | S | S | S | S | D | S | + | + | M | W |  |  |  |  |  |  |  |  |  |  | 2 |
| daddui r1,r1,8 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | S | D | E | S | M | W |  |  |  |  |  |  |  |  |  | 1 |
| daddi r2,r2,-1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | D | S | E | M | W |  |  |  |  |  |  |  |  | 1 |
| bnez r2,loop |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | S | S | D | E | M | W |  |  |  |  |  |  | 2 |
| Halt |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | - | - | - | - |  |  |  |  |  | 1 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 25\*100+6 = 2506 |
| TOTAL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Domanda 2**

Considerando il programma precedente, calcolare la miss prediction ratio per i seguenti casi:

* + - 1. processore con predittore di salti statico di tipo always taken

1/100

* + - 1. processore con predittore di salti statico di tipo always not taken

99/100

* + - 1. processore con predittore di salti dinamico di tipo BHT di 2-bit con 1024 linee, con tutti i predittori inizializzati a 0.

**3/100**

**Domanda 3**

Considerando il programma precedente e l’architettura del processore superscalare descritto in seguito; completare la tabella relativa alle prime 3 iterazioni.

Processor architecture:

* + Issue 2 instructions per clock cycle
  + jump instructions require 1 issue
  + handle 2 instructions commit per clock cycle
  + timing facts for the following separate functional units:
    1. 1 Memory address 1 clock cycle
    2. 1 Integer ALU 1 clock cycle
    3. 1 Jump unit 1 clock cycle
    4. 1 FP multiplier unit, which is pipelined: 6 stages
    5. 1 FP divider unit, which is not pipelined: 6 clock cycles
    6. 1 FP Arithmetic unit, which is pipelined: 2 stages
  + Branch prediction is always correct
  + There are no cache misses
  + There are 2 CDB (Common Data Bus).

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| # iteration |  | Issue | EXE | MEM | CDB x2 | COMMIT x2 |
| 1 | l.d f1,v1(r1) | 1 | 2ea | 3 | 4 | 5 |
| 1 | l.d f2,v2(r1) | 1 | 3ea | 4 | 5 | 6 |
| 1 | mul.d f4,f1,f2 | 2 | 6-11m | - | 12 | 13 |
| 1 | l.d f3,v3(r1) | 2 | 4ea | 5 | 6 | 13 |
| 1 | mul.d f4,f4,f3 | 3 | 13-18m | - | 19 | 20 |
| 1 | s.d f4,v4(r1) | 3 | 5ea | - | - | 20 |
| 1 | add.d f5,f1,f3 | 4 | 7-8a | - | 9 | 21 |
| 1 | s.d f5,v5(r1) | 4 | 6ea | - | - | 21 |
| 1 | daddui r1,r1,8 | 5 | 6i | - | 7 | 22 |
| 1 | daddi r2,r2,-1 | 5 | 7i | - | 8 | 22 |
| 1 | bnez r2,loop | 6 | 9j | - | - | 23 |
| 2 | l.d f1,v1(r1) | 7 | 8ea | 9 | 10 | 23 |
| 2 | l.d f2,v2(r1) | 7 | 9ea | 10 | 11 | 24 |
| 2 | mul.d f4,f1,f2 | 8 | 12-17 m | - | 18 | 24 |
| 2 | l.d f3,v3(r1) | 8 | 10ea | 11 | 12 | 25 |
| 2 | mul.d f4,f4,f3 | 9 | 19-24m | - | 25 | 26 |
| 2 | s.d f4,v4(r1) | 9 | 11ea | - | - | 26 |
| 2 | add.d f5,f1,f3 | 10 | 13-14a | - | 15 | 27 |
| 2 | s.d f5,v5(r1) | 10 | 12ea | - | - | 27 |
| 2 | daddui r1,r1,8 | 11 | 12i | - | 13 | 28 |
| 2 | daddi r2,r2,-1 | 11 | 13i | - | 14 | 28 |
| 2 | bnez r2,loop | 12 | 15j | - | - | 29 |
| 3 | l.d f1,v1(r1) | 12 | 13ea | 14 | 15 | 29 |
| 3 | l.d f2,v2(r1) | 13 | 14ea | 15 | 16 | 30 |
| 3 | mul.d f4,f1,f2 | 13 | 17-22 m | - | 23 | 30 |
| 3 | l.d f3,v3(r1) | 14 | 15ea | 16 | 17 | 31 |
| 3 | mul.d f4,f4,f3 | 14 | 24-29m | - | 30 | 31 |
| 3 | s.d f4,v4(r1) | 15 | 16ea | - | - | 32 |
| 3 | add.d f5,f1,f3 | 15 | 18-19a | - | 20 | 32 |
| 3 | s.d f5,v5(r1) | 16 | 17ea | - | - | 33 |
| 3 | daddui r1,r1,8 | 16 | 17i | - | 18 | 33 |
| 3 | daddi r2,r2,-1 | 17 | 18i | - | 19 | 34 |
| 3 | bnez r2,loop | 18 | 20j | - | - | 35 |

**Domanda 4**

Considerando il segmento di codice presentato nella tabella precedente, se assumiamo che ci sia un unico Common Data Bus, qual è la prima istruzione che dovrebbe stallare durante l’esecuzione del programma? motivare la risposta.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 2 | l.d f3,v3(r1) | 8 | 10ea | 11 | 12 | 25 |